DASIP 2025: Workshop on Design and Architectures for Signal and Image Processing

in conjunction with the 20th HiPEAC Conference in Barcelona, Spain, January 20-22, 2025.

Chairs

Ahmed Kamaleldin, Technical University Dresden - DE

Jordane Lorandel, Université de Rennes – IETR – CNRS-FR

CALL FOR PAPERS

The **Workshop on Design and Architectures for Signal and Image Processing (DASIP)** provides an inspiring international forum for the latest innovations and developments in the field of leading signal, image and video processing and machine learning in custom embedded, edge and cloud computing architectures and systems. The workshop program will include keynote speeches and contributed paper sessions. The 18th edition will be held in conjunction with the 20th HiPEAC Conference in Barcelona, Spain, January 20-22, 2025.

SUBMISSION GUIDELINES

Authors should submit their full papers (up to 12 pages) and/or short papers (up to 6 pages, intended for work-in-progress with promising results and/or students at the early stages of their research) in the single-column Springer LNCS format in PDF through the Easy Chair system.

Submitted papers are required to describe original unpublished work and must not be under consideration for publication elsewhere. Submissions must be fully anonymous, but authors should not hide previous work, instead, they need to make self-references in the third person. More details on submission requirements, templates and submission instructions are provided on the DASIP website.

Each submission will receive at least three independent double blind reviews from the members of our scientific committee. Authors are encouraged to take the reviewers' comments into account when they prepare the final versions of their papers and present the research during the workshop prior to its publication. The conference proceedings will be published in the Springer LNCS Series, on the Springer Link website. Paper and keynote presentation slides and tutorial documents will be made available to workshop attendees after the workshop (subject to confidentiality issues).

Authors of best papers of DASIP'2024 and DASIP'2025 will be invited to submit an extended version of their work to a Special Issue in Elsevier's Journal of System Architecture (JSA).

IMPORTANT DATES (ALL 23:59 A.O.E)

- Paper submission deadline: **October 14th, 2024**
- Notification of acceptance: November 25th, 2024
- Camera ready papers: December 2nd, 2024
- Workshop: January 20-22, 2025

VENUE

The Workshop on Design and Architectures for Signal and Image Processing will be held in conjunction with the 20th HiPEAC Conference in Barcelona, Spain, January 20-22, 2025.

Registration

DASIP 2025 is a HiPEAC-based workshop. Hence, a registration at HiPEAC is required. Please be aware that for each accepted paper, at least, one of the authors must pay the full registration fee in order for the paper to be included in the workshop proceedings and scheduled in the program.

CONTACT

All questions about the workshop and submissions should be emailed to Ahmed Kamaleldin <ahmed.kamal@tu-dresden.de> or Jordane Lorandel <jordane.lorandel@univ-rennes.fr>.

LIST OF TOPICS

Prospective authors are invited to submit manuscripts on topics including, but not limited to:

Custom embedded, edge and cloud architectures and systems:

- Machine learning and deep learning architectures for inference and training
- Systems for autonomous vehicles : cars, drones, ships and space applications
- Image processing and compression architectures
- Smart cameras, security systems, behaviour recognition
- Edge and cloud processing: special routing, configurable co-processors and low energy considerations
- Real-time cryptography, secure computing, financial and personal data processing
- Computer arithmetic, approximate computing, probabilistic computing, nanocomputing, bio-inspired computing
- Biological data collection and analysis, bioinformatics
- Personal digital assistants, natural language processing, wearable computing and implantable devices
- Global navigation satellite and inertial navigation systems

Design Methods and Tools:

- Design verification and fault tolerance
- Embedded system security and security validation
- System-level design and hardware/software co-design
- High-level synthesis, logic synthesis, communication synthesis
- Embedded real-time systems and real-time operating systems
- Rapid system prototyping, performance analysis and estimation
- Formal models, transformations, algorithm transformations and metrics

Development Platforms, Architectures and Technologies:

- Embedded platforms for multimedia and telecommunication
- Many-core and multi-processor systems, SoCs, and NoCs
- Reconfigurable ASIPs, FPGAs, and dynamically reconfigurable systems
- Memory system and cache management
- Asynchronous (self-timed) circuits and analog and mixed-signal circuits

STEERING COMMITTEE

- Alfonso Rodríguez, Universidad Politécnica de Madrid, Madrid, Spain
- Diana Goehringer, TU Dresden
- Jean-Pierre David, Ecole Polytechnique de Montreal
- Joao M. P. Cardoso, University of Porto
- Marek Gorgon, AGH University of Science and Technology
- Miguel Chavarrías, Universidad Politécnica de Madrid, Madrid, Spain
- Michael Huebner, Brandenburg University of Technology
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- Sebastien Pillement, University of Nantes - IETR